What is claim d is:

1. A semiconductor memory device, comprising:

an isolation controller applying a drive control signal for driving an isolation part at a internal supply voltage level lower than a specified high voltage level, after lapse of a given time from a precharge starting time point of an equalizer.

2. The device of claim 1, wherein the lapse of given time occurs while the equalizer is in a precharge mode.

3. The device of claim 1, wherein the isolation controller includes:

an isolation control signal generator applying the drive control signal to the isolation part; and

a control signal delay delaying the drive control signal for lapse of the given time.

4. The device of claim 3, wherein

in an active mode, the drive control signal is applied as a high voltage level to an isolation part connected to a selected memory cell, and is applied as a ground voltage level to an isolation part connected to a non-selected memory cell, and

in a precharge mode, the drive control signal is applied at the internal supply voltage level to isolation parts connected to the selected and non-selected memory cells.

5. The device of claim 3, wherein the control signal delay includes at least one of an RC delay and an inverter chain.

6. The device of claim 1, wherein the isolation part includes at least a pair of N-type MOS transistors, each having a threshold voltage higher than transistors receiving the internal supply voltage level through a gate thereof.

7. The device of claim 3, wherein the isolation control signal generator includes:

a NAND gate receiving operation mode signals to generate a NAND response for output as an enable signal;

a plurality of P-type MOS transistors equalizing a drive control signal line pair in response to a first state of the enable signal, and enabling a high voltage level difference between signal lines of the drive control signal line pair in response to a second state of the enable signal; and

an N-type MOS transistor connected to a common access node of at least one of the plurality of P-type MOS transistors, for supplying the internal supply voltage level.

8. A semiconductor memory device, comprising:

a memory cell array configured as a plurality of memory cell blocks of memory cells, the memory cells connected to one another at points crossed between a plurality of word lines and a plurality of bitlines;

a sense amplifier connected to the memory cells via a bitline pair;

an isolation part connected to the bitline pair for electrically connecting a memory cell to, or isolating the memory cell from, the sense amplifier;an equalizer connected to the bitline pair between the isolation part and a memory cell block for precharging, in a precharge mode, each bitline of the bitline pair to the same voltage;an isolation control signal generator applying an isolation control signal to the isolation part; and

a control signal delay delaying the isolation control signal for a given time from a precharge starting time point of the equalizer,

the isolation control signal generator applying the isolation control signal at an internal supply voltage level that is lower than a specified high voltage level.

9. The device of claim 8, wherein, in the precharge mode, the isolation control signal is applied as the internal supply voltage level to at least one isolation part individually connected to one or more memory cell blocks.

10. The device of claim 8, wherein

in an active mode, the isolation control signal is applied as a high voltage level to an isolation part connected to a selected memory cell, and is

applied as a ground voltage level to an isolation part connected to a non-selected memory cell, and

in the precharge mode, the isolation control signal is applied as the internal supply voltage level to isolation parts connected to the selected and non-selected memory cells.

11. The device of claim 8, wherein the control signal delay includes at least one of an RC delay and an inverter chain.

12. The device of claim 8, wherein the isolation control signal generator includes:

a NAND gate for receiving operation mode signals to generate an enable signal at an output thereof;

first, second and third P-type MOS transistors equalizing an isolation control signal line pair in response to a first state of the enable signal, and enabling a high voltage level difference between signal lines of the drive control signal line pair in response to a second state of the enable signal; and

an N-type MOS transistor connected to a common access node of the second and third P-type MOS transistors, for supplying the internal supply voltage.

13. The device of claim 12, wherein the control signal delay includes an RC delay connected to the NAND gate, and at least two resistors, each connected to a source and a drain of the first P-type MOS transistor.

14. The device of claim 12, wherein the control signal delay includes an inverter chain of even-numbered terminals connected to the NAND gate output.

15. The device of claim 8, wherein the memory cells are configured in a matrix structure.

16. The device of claim 8, wherein

a memory cell is connected to, or isolated from, the sense amplifier

based on a state of the isolation control signal applied thereto; and

the equalizer precharges the bitlines in response to a state of an equalization control signal applied thereto.

17. A method of accelerating a precharge time in a semiconductor memory device, comprising:

applying an equalization enable signal to an equalizer at initiation of a precharge mode to precharge a bitline pair connecting a memory cell block to a sense amplifier; and

delaying isolation control signals by a given time in the precharge mode, and

applying the isolation control signals to isolation parts adapted to connect the memory cell block to or isolate the memory cell block from the sense amplifier, so that a time of applying the isolation control signals is after a time of applying the equalization enable signal.

18. The method of claim 17, wherein, in the precharge mode, an isolation control signal applied to an isolation part connected to a selected memory cell block, and an isolation control signal applied to an isolation part connected to a non-selected memory cell block are applied at the same internal supply voltage level.

19. The method of claim 18, wherein, in an active mode

the isolation control signal applied to the isolation part connected to the selected memory cell block is at a high voltage level, and

the isolation control signal applied to the isolation part connected to the non-selected memory cell block is at a ground voltage level.

20. A memory device having an isolation part electrically connecting a memory cell to, or isolating the memory cell from, a sense amplifier via a bitline pair, the device including an equalizer for precharging, in a precharge mode, each bitline of the bitline pair to the same voltage, comprising:

an isolation controller for applying, during the precharge mode, a voltage at a level substantially similar to a specified high voltage level to a

gate of an isolation transistor of the isolation part that is connected to at least one bitline of the bitline pair, and for applying an internal supply voltage at a level lower than the specified high voltage level during the precharge mode.

21. The device of claim 20, wherein the voltage substantially similar to a specified high voltage level is applied earlier in time during the precharge mode than the applied internal supply voltage.

22. A semiconductor memory device accelerating a precharge time therein in accordance with the method of claim 17.

23. A memory device having an isolation part electrically connecting a memory cell to, or isolating the memory cell from, a sense amplifier via a bitline pair, the device including an equalizer for precharging, in a precharge mode, each bitline of the bitline pair to the same voltage, the memory device accelerating a precharge time therein in accordance with the method of claim 17.